Notice of Allowability	Application No.	Applicant(s)	
	09/921,293	CLARKE ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Response filed 24 May 2005*.

2. ☒ The allowed claim(s) is/are *1-21,29,34-40,42 and 43*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

HAL WACHSMAN
PRIMARY EXAMINER

DETAILED ACTION

Information Disclosure Statement

1. The following references, originally listed on the Information Disclosure Statement filed February 24, 2004, have been timely submitted by Applicant and considered by the Examiner:

William F. Egan, "Chapter 9: Acquisition Aids," Phase-Lock Basics, John Wiley & Sons, Inc., 1998, pp. 209-210 and 222-227.

"General Metrology --- Part 3: Guide to the Expression of Uncertainty in Measurement (GUM)," Published Document PD 6461-3:1995, British Standards, January 15, 1995, pp. 1-105.

Drawings

2. The drawing changes filed on July 11, 2003, and January 12, 2004 have been accepted by the Examiner. Applicant is required to submit a formal set of drawings including the proposed changes indicated in the drawings filed July 11, 2003.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. Authorization for this examiner's amendment was given in a telephone interview with Mr. Brian Dorini on June 21, 2005.

5. The application has been amended as follows:

In claim 1, line 6, "loop;" has been changed to ---loop, wherein the second phase-locked loop includes a center frequency input, and the center frequency input is coupled to the first output signal to assist lock-in by the second phase-locked loop;---

In claim 9, line 1, "The process variable transmitter of claim 8 further comprising" has been changed to ---A process variable transmitter, comprising: a first phase-locked loop having a first bandwidth producing a first output signal, and operable to lock into a frequency of an input signal; a second phase-locked loop having a second bandwidth narrower than the first bandwidth, producing a second output signal, and operable to lock into the frequency of the input signal with greater accuracy and greater immunity to noise than the first phase-locked loop; a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency; an amplitude detector operable to sense an amplitude of the input signal and to

generate a low flow signal when the amplitude of the input signal is below a user-controlled value; and---.

In claim 14, line 10, "signal, and" has been changed to ---signal, at least one of the PLLs having a center frequency input coupled to a PLL output signal of another of the PLLs to assist lock-in by the at least one PLL, and---.

In claim 21, line 17, "input signal; and" has been changed to ---input signal;---.

In claim 21, line 20, "input signal." has been changed to ---input signal; and providing the output signal of the first PLL to the second PLL as a center frequency of the second PLL to assist lock-in by the second PLL.---.

Claim 23 has been cancelled.

Claim 28 has been cancelled.

In claim 38, line 10, "sensor signal, and" has been changed to ---sensor signal, at least one of the PLLs having a center frequency input coupled to a PLL output signal of another of the PLLs to assist lock-in by the at least one PLL, and---.

In claim 38, line 12, "output signals;" has been changed to ---output signals, based on one or more lock indicator signals;---.

In claim 43, line 1, "The process variable transmitter of claim 1" has been changed to ---A process variable transmitter, comprising: a first phase-locked loop having a first bandwidth producing a first output signal, and operable to lock into a frequency of an input signal; a second phase-locked loop having a second bandwidth narrower than the first bandwidth, producing a second output signal, and operable to lock into the frequency of the input signal with greater accuracy and

greater immunity to noise than the first phase-locked loop; and a switch operable to switch an output signal of the process variable transmitter between the first output signal and the second output signal in response to a change in the frequency, and based on at least one of a first lock indicator signal and a second lock indicator signal, wherein the fist lock indicator signal indicates whether the first phase-locked loop is locked into the frequency and the second lock indicator signal indicates whether the second phase-locked loop is locked into the frequency,---.

Allowable Subject Matter

6. Claims 1-21, 29, 34-40, 42, and 43 are considered to be allowable over the cited prior art for the following reasons:

Egan et al, "Phase-Lock Basics" discloses a first phase-locked loop having a first bandwidth producing a first output signal, and operable to lock into a frequency of an input signal (page 222, 9.2.1), modifying the characteristics of the phase-locked loop to form a second phase-locked loop having a second bandwidth narrower than the first bandwidth, producing a second output signal, and operable to lock into the frequency of the input signal (page 223-224, 9.2.2). Egan also discloses a switch operable to switch the bandwidth of the phase locked loop, and correspondingly switch the output of the phase-locked loop, between the first output signal and the second output signal in response to a change in the frequency and based on a first lock indicator signal wherein the first lock indicator signal indicates whether the first phase-locked loop is locked into the frequency (page 223-224, 9.2.2).

U.S. Patent No. 3,751,979 to Ims.Ims teaches a process variable transmitter (i.e. flow speed measurement system) (column 1, lines 29-30) including two separate phase locked loops (column 16, lines 6-8) and a switch operable to switch the output of the process variable transmitter between a first output of the first phase locked loop and a second output of the second phase locked loop (column 16, lines 26-29 and Figure 8)

U.S. Patent No. 4,463,612 to Thompson discloses an electronic circuit using digital techniques for vortex shedding flowmeter signal processing comprising a vortex flow sensor (i.e. process variable transmitter) that produces a signal over a line, which varies with the vortex shedding frequency, to a preamplifier, and then over an A.C. coupling to a phase detector (column 2, lines 63-66). Thompson discloses a phase lock loop (column 3, lines 1-4) comprising a phase detector that receives the input signal and produces an output signal to a low-pass loop filter that outputs a filtered signal to a voltage controlled oscillator that feeds-back a locking oscillator signal to the phase detector (Figure 1). Thompson also discloses including the components of the system on a single low-power digital signal processor chip used for use in a software process (column 3, lines 39-43 and 61-62). Thompson discloses including an amplitude detector (i.e. drop out detector) that senses the amplitude of the input signal and generates a low flow signal when it is below a predetermined level (column 2, lines 13-19).

U.S. Patent No. 5,493,915 to Lew et al. teaches a fluid dynamic torsional vortex sensor including a data processor that receives the alternating electrical signal and determines the flow rate with a low flow condition producing a signal with a small amplitude (column 5, lines 9-18).

U.S. Patent No. 5,576,497 to Vignos et al. teaches adaptive filtering for a vortex flowmeter including a well known vortex sensor that produces an analog sinusoidal signal representative of the alternating differential pressure various to calculate fluid flow or velocity (column 2, lines 44-49). Vignos also teaches an initial signal conditioner which filters the signal before subsequent processing occurs (column 2, lines 49-57).

U.S. Patent No. 6,298,100 to Bouillet teaches a phase error estimation method for a demodulator comprising a phase locked loop with a pilot component as a reference and a conventional phase detector for phase acquisition, all part of a phase control loop (column 3, lines 13-17). Bouillet also teaches including a Hilbert filter for receiving the pilot signal, transforming the signal into in-phase and quadrature components, and applying the transformed components to the phase control loop (column 3, lines 31-46). Bouillet also teaches heterodyning the reference pilot with the carrier in the main path of the phase locked loop (column 4, lines 15-30).

U.S. Patent No. 5,570,300 to Henry et al. teaches self-validating sensors, using software (column 14, lines 40-41), that include a transducer for generating a data signal related to the value of a variable and a transmitter for receiving the data signal and generating output signals, wherein the transmitter generates a first output signal related to the value of the variable and a second output based on a dynamic uncertainty analysis of the first output signal (abstract). Henry also teaches that the uncertainty parameters include a measurement status variable (column 2, lines 17-20) indicating quality (column 7, lines 60-63) based upon the varying frequency of the output signal (column 9, lines 14-27 and column 13, line 61 to column 14, line 22).

U.S. Patent No. 4,201,084 to Ito et al. teaches a vortex flow meter including a filter switchable between active and inactive states (column 2, lines 10-24) wherein the filter is active when a low flow condition exists (column 7, lines 12-21).

U.S. Patent No. 5,128,625 to Yatsuzuka et al. teaches an adaptive phase lock loop system comprising two phase locked loops prepared so that the first PLL caries out on the initial training mode, and the second PLL performs the conventional process so that when the PLLs are initially or periodically initiated, the second PLL is activated with the initial phase and center frequency given by the first PLL after the initial training mode is performed (column 14, lines 14-20).

The following newly discovered references are considered pertinent to the examination of the Application.

U.S. Patent Application Publication No. 2001/0008384 to Ku teaches a method for generating frequencies in a Dual Phase Locked Loop.

U.S. Patent No. 5,502,711 to Clark et al. teaches a dual digital phase locked loop clock channel for optical recording.

U.S. Patent No. 5,414,390 to Kovacs et al. teaches a center frequency controlled phase locked loop system.

U.S. Patent No. 6,438,177 to Ikeda teaches a digital satellite broadcasting receiver in which loop bandwidth of a PLL circuit is changed at the time of centering.

U.S. Patent No. 5,152,005 to Bickley teaches high resolution frequency synthesis using dual phase locked loops.

U.S. Patent No. 5,072,195 to Graham et al. teaches a phase-locked loop with clamped voltage-controlled oscillator.

U.S. Patent No. 4,019,153 to Cox, Jr. et al. teaches a digital phase-locked loop filter including a dual phase locked loop arrangement for center frequency adjustment.

U.S. Patent No. 5,029,004 to Shibayama teaches an edge enhancement apparatus useful with liquid crystal displays including a dual phase locked loop arrangement for center frequency adjustment.

Claims 1, 14, 21, 38, and 43 are considered to be allowable over the cited prior art because while the cited prior art does teach many of the features of the claimed invention, none of the cited prior art teaches or suggests, in combination with the other claimed limitations for a process variable transmitter/vortex flowmeter, first and second phase locked loops both operable to lock into the frequency of the same input signal and generate corresponding output signals and a switching means for switching an output signal of the process variable transmitter/vortex flowmeter from among the PLL output signals based on one or more lock indicator signals, wherein at least one of the PLLs has a center frequency input coupled to a PLL output signal of another of the PLLs to assist lock-in by the at least one PLL.

Further, while the invention of Yatsuzuka does teach an adaptive phase lock loop system comprising two phase locked loops prepared so that the first PLL caries out on the initial training mode, and the second PLL performs the conventional process so that when the PLLs are initially or periodically initiated, the second PLL is activated with the initial phase and center frequency given by the first PLL after the initial training mode is performed (column 14, lines 14-20), Yatsuzuka specifically indicates that the training PLL is used only in training operation and does not add to the operation of the system under normal conditions. Therefore, the invention of Yatsuzuka teaches away from any combination with the invention of Egan and Ims which, in accordance with the claimed invention, requires switching the output of the variable process transmitter/vortex flowmeter among the outputs of the PLLs, including the PLL assisting in lock-in.

Claims 9 and 39 are considered to be allowable over the cited prior art because while the cited prior art does teach a switchable pre-filter the cited prior art does not indicate that this switchable pre-filter replaces the inputs to a PLL when it is on or that the first output signal is applied as a fixed center frequency of the second phase locked loop. Therefore, none of the cited prior art teaches or suggests, in combination with the other claimed limitations for a process variable transmitter, a pre-filter wherein, based on a status of the low-flow signal, a fixed center frequency of the second phase-locked loop switchable between an output signal of a first phase-locked loop, and $2\pi f_{ph}$, where f_{ph} is a high cut-off frequency of the pre-filter and the switch switches the output of the process variable transmitter to the second output signal.

Claim 40 is considered to be allowable over the cited prior art because while the cited prior art does teach a self-validating module that includes status variables of CLEAR, BLURRED, DAZZLED, and BLIND, none of the cited prior art teaches or suggests, in combination with the other claimed limitations for a signal processing apparatus, specifying that the measurement status variable of the self-validating module be CLEAR when both lock indicator signals indicate lock, BLURRED when one of the two lock indicator signals indicates lock and the other of the two lock indicator signals indicates no lock, DAZZLED when both lock indicator signals

indicate no lock, and BLIND when both lock indicator signals indicate no lock for at least a predetermined length of time.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
June 23, 2005

HAL WACHSMAN
PRIMARY EXAMINER